



# STIC Search Report

EIC 2800

STIC Database Tracking Number: 129223

**TO:** Monica Lewis  
**Location:**  
**Art Unit :** 2822  
**Tuesday, August 10, 2004**  
**Case Serial Number:** 10/010237

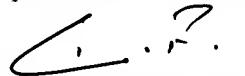
**From:** Bode Fagbohunka  
**Location:** EIC 2800  
**Jeff 4A58**  
**Phone:** 571-272-2541  
**bode.fagbohunka@uspto.gov**

## Search Notes

Examiner Monica Lewis

Please find attached the results of your search for 10/010237. The search was conducted using the standard collection of databases on dialog for EIC 2800. The tagged references appear to be the closest references located during our search.

If you would like a re-focus please let me know or if you have any questions regarding the search results please do not hesitate to contact me.

  
Bode Fagbohunka



# STIC Search Results Feedback Form

EIC 2800

Questions about the scope or the results of the search? Contact *the EIC searcher or contact:*

Jeff Harrison, EIC 2800 Team Leader  
571-272-2511, JEF 4B68

## Voluntary Results Feedback Form

➤ I am an examiner in Workgroup:

Example: 2810

➤ Relevant prior art found, search results used as follows:

- 102 rejection
- 103 rejection
- Cited as being of interest.
- Helped examiner better understand the invention.
- Helped examiner better understand the state of the art in their technology.

Types of relevant prior art found:

- Foreign Patent(s)
- Non-Patent Literature  
(journal articles, conference proceedings, new product announcements etc.)

➤ Relevant prior art not found:

- Results verified the lack of relevant prior art (helped determine patentability).
- Results were not useful in determining patentability or understanding the invention.

Comments:

Drop off or send completed forms to STIC/EIC 2800, CPTA-3018



Set	Items	Description
S1	2198733	CAPACIT?????
S2	114142	WINDOW()FRAM? OR WINDOWFRAM? OR UNI
S3	4951098	IC? ? OR WAFER? OR SEMICONDUCT? OR SEMI()CONDUCT? OR PACKA-
	G?	G?
S4	579047	(BOTTOM? OR UPPER? OR TOP? ? OR FIRST? OR SECOND?) (3N) SURF-
	ACE?	ACE?
S5	9807494	APERTURE? OR ORIFICE? OR SPACE? OR OPEN? OR HOLE? OR GAP?
S6	191086	POWER (6N) CONNECT?
S7	21903	BGA? ? OR BALL (2N) ARRAY
S8	112893	UNITAR???????
S9	158	(S2 OR S8) (2N) S1
S10	0	S9 AND S4 AND S5 AND S6 AND S7
S11	1	S9 AND S4
S12	27	S9 AND (S5 OR S6 OR S7)
S13	26	S12 NOT S11
S14	23	RD (unique items)
S15	208	S8 (6N) S1
S16	1	S15 AND (S4 OR S5) AND S6
S17	0	S16 NOT S14
S18	75	S15 AND (S4 OR S5)
S19	0	S18 AND S7
S20	7	S18 AND S3
S21	7	RD (unique items)
S22	0	S15 AND S7
S23	1	S15 AND S6
S24	84	S1 (2N) S8
S25	17	S24 AND POWER?
S26	13	RD (unique items)
S27	8	S24 AND (S3 OR DIE? ?)
S28	6	RD (unique items)
S29	5	S28 NOT S26
? show files		
File	2:INSPEC 1969-2004/Aug W1	
	(c) 2004 Institution of Electrical Engineers	
File	6:NTIS 1964-2004/Aug W2	
	(c) 2004 NTIS, Intl Cpyrgh All Rights Res	
File	8:Ei Compendex(R) 1970-2004/Aug W1	
	(c) 2004 Elsevier Eng. Info. Inc.	
File	34:SciSearch(R) Cited Ref Sci 1990-2004/Aug W2	
	(c) 2004 Inst for Sci Info	
File	434:SciSearch(R) Cited Ref Sci 1974-1989/Dec	
	(c) 1998 Inst for Sci Info	
File	99:Wilson Appl. Sci & Tech Abs 1983-2004/Jul	
	(c) 2004 The HW Wilson Co.	
File	94:JICST-EPlus 1985-2004/Jul W3	
	(c) 2004 Japan Science and Tech Corp (JST)	
File	92:IHS Intl.Stds. & Specs. 1999/Nov	
	(c) 1999 Information Handling Services	
File	144:Pascal 1973-2004/Aug W1	
	(c) 2004 INIST/CNRS	
File	647:CMP Computer Fulltext 1988-2004/Aug W1	
	(c) 2004 CMP Media, LLC	
File	696:DIALOG Telecom. Newsletters 1995-2004/Aug 11	
	(c) 2004 The Dialog Corp.	
File	35:Dissertation Abs Online 1861-2004/May	
	(c) 2004 ProQuest Info&Learning	
File	65:Inside Conferences 1993-2004/Aug W2	
	(c) 2004 BLDSC all rts. reserv.	
File	103:Energy SciTec 1974-2004/Jul B2	

(c) 2004 Contains copyrighted material  
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200451  
(c) 2004 Thomson Derwent  
File 347:JAPIO Nov 1976-2004/Apr (Updated 040802)  
(c) 2004 JPO & JAPIO  
File 202:Info. Sci. & Tech. Abs. 1966-2004/Jul 12  
(c) 2004 EBSCO Publishing  
File 239:Mathsci 1940-2004/Sep  
(c) 2004 American Mathematical Society  
File 95:TEME-Technology & Management 1989-2004/Jun W1  
(c) 2004 FIZ TECHNIK  
File 25:Weldasearch 1966-2003/Dec  
(c) 2004 TWI Ltd  
File 62:SPIN(R) 1975-2004/Jun W2  
(c) 2004 American Institute of Physics  
File 96:FLUIDEX 1972-2004/Aug  
(c) 2004 Elsevier Science Ltd.  
File 98:General Sci Abs/Full-Text 1984-2004/Jul  
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File 266:FEDRIP 2004/Jun  
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11/9/1 (Item 1 from file: 350)  
DIALOG(R) File 350:Derwent WPIX  
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013177720 \*\*Image available\*\*  
WPI Acc No: 2000-349593/200030  
Related WPI Acc No: 2000-349452; 2003-165492; 2003-439432  
XRAM Acc No: C00-106267  
XRPX Acc No: N00-261920

**Formation of a semiconductor structure for a semiconductor device**  
**includes forming a refractory metal within the recess, forming refractory**  
**metal nitride layers and forming a metallization layer to fill the recess**

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)

Inventor: GIVENS J H; KRAUS B D; ZAHORIK R C

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6057231	A	20000502	US 97942811	A	19971002	200030 B
			US 99248499	A	19990210	

Priority Applications (No Type Date): US 97942811 A 19971002; US 99248499 A 19990210

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6057231	A	15	H01L-021/44	Div ex application	US 97942811

Abstract (Basic): US 6057231 A

NOVELTY - A semiconductor structure (10) is formed by forming a) a recess in the dielectric layer (14) on a substrate; b) a refractory metal layer (24) in the recess; c) a first refractory metal nitride layer (26) on the metal layer then heat treating the semiconductor substrate (12); d) a second refractory metal nitride layer (32) on the first; and e) a metallization layer to fill the recess.

USE - For forming a high aspect-ratio contact in a semiconductor device.

ADVANTAGE - The method forms a high aspect ratio structure that allows for taller microelectronic component i.e. taller stacked dynamic random access memory (DRAM) capacitor, where the interconnect to the stacked DRAM capacitor is unitary and formed by a single recess filling process.

DESCRIPTION OF DRAWING(S) - The figure shows an elevational cross-section illustration of the recess filling.

Semiconductor structure (10)  
Semiconductor substrate (12)  
Dielectric layer (14)  
Refractory metal layer (24)  
First refractory metal nitride layer (26)  
Second refractory metal nitride layer (32)  
pp; 15 DwgNo 6/7

Technology Focus:

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Method: Forming the refractory metal layer is conducted by a titanium chemical vapor deposition (CVD) process. Forming the second refractory metal nitride layer is conducted by a titanium nitride physical vapor deposition (PVD) process that causes titanium nitride to impact upon the first refractory metal layer nitride at an angle that is orthogonal to the plane of the semiconductor substrate. The step of forming a metallization layer further comprises depositing an aluminum alloy composition to cover the recess at a deposition energy of 0.5-5 kW, preferably 5-20 kW and at 400-600degreesC, preferably 450-650degreesC; and applying for 1-500 seconds a pressure of 450-1,050 atmospheres and

a temperature of 100-700degreesC. Heat treating step is conducted at 100-660degreesC for 10-60 seconds. Treating the semiconductor substrate with ammonia is conducted while heating the substrate at 100-500degreesC, preferably greater 200-400degreesC. The precleaning is conducted at 100:1 aqueous HF dip for 30 seconds. Preferred Property: The titanium nitride layer formed is 1,500-2,500 Angstrom, preferably 100-500 Angstrom thick. The layer of aluminum or aluminum alloy is 1.0-2.0um, preferably 0.5-2.0 um. The refractory metal layer is 100-300Angstrom thick. Preferred Compound: The titanium nitride CVD process uses tetrakis (dimethylamino) titanium (TDMAT) or trimethylethylenediamine tris (dimethylamino) titanium (TMEDT).

ELECTRONICS - Preferred Property: The recess has a height to width ratio of 6:1-10:1 and an opening of at most 0.35 mum at a top surface of the dielectric layer. The width of the trench opening wider or at most that of the contact hole opening and the length of the trench is parallel to the semiconductor substrate that exceeds the width of the contact hole opening. Preferred Method: Heat treating is conducted by rapid thermal processing (RTP) annealing.

Extension Abstract:

EXAMPLE - In an EMBODIMENT of the invention, the method includes performing a precleaning operation by subjecting the substrate to a hydrogen fluoride (HF) composition, and performing a degassing operation by subjecting the substrate to a vacuum. A first refractory metal nitride layer is formed within the recess upon the refractory metal layer by a titanium nitride CVD process using trimethylethylenediamine tris (dimethylamine) titanium (TMEDT). The substrate is treated with ammonia to replace interstitial impurities in the refractory metal nitride layer with nitrogen.

Title Terms: FORMATION; SEMICONDUCTOR; STRUCTURE; SEMICONDUCTOR; DEVICE; FORMING; REFRACTORY; METAL; RECESS; FORMING; REFRACTORY; METAL; NITRIDE; LAYER; FORMING; METALLISE; LAYER; FILL; RECESS

Derwent Class: L03; U11

International Patent Class (Main): H01L-021/44

International Patent Class (Additional): H01L-021/44

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L04-C10F

Manual Codes (EPI/S-X): U11-C05

Derwent Registry Numbers: 1712-U; 1713-U; 1738-U

?

21/9/5 (Item 3 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
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011684441 \*\*Image available\*\*  
WPI Acc No: 1998-101351/199809

XRPX Acc No: N98-081198

Unitary packaging system for capacitor and inductor - places capacitor in ferrite shell, and forms winding around shell to provide inductive component

Patent Assignee: MOTOROLA INC (MOTI )

Inventor: CHASON M; GOEL S; HARSHE G R; KEYVANI D; NERZ J E

Number of Countries: 019 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 9801947	A1	19980115	WO 97US10860	A	19970702	199809 B
US 5838214	A	19981117	US 96676611	A	19960708	199902

Priority Applications (No Type Date): US 96676611 A 19960708

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

WO 9801947 A1 E 13 H03H-007/09

Designated States (National): JP

Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LU MC  
NL PT SE

US 5838214 A H03H-007/09

Abstract (Basic): WO 9801947 A

The system includes a capacitor with electrical contacts. There is an device for holding the capacitor, such that the electrical contacts extend beyond the holding device. An electric current carrying part has a least one turn wound around the holding device, to form an inductive component. This may include a primary and a secondary winding. The capacitor is preferably and electrochemical capacitor (14).

The holding device containing the capacitor comprises a magnetic flux storing material, which is preferably ferrite, or may be several ferrous plates. The holder may be formed as a toroidal shell arrangement, in which the capacitor electrical contacts extend through the shell.

ADVANTAGE - Space efficient and increases assembly efficiency, decreasing handling time.

Dwg.2/4

Title Terms: UNIT; PACKAGE ; SYSTEM; CAPACITOR; INDUCTOR; PLACE; CAPACITOR ; FERRITE; SHELL; FORM; WIND; SHELL; INDUCTIVE; COMPONENT

Derwent Class: U25; V01; V02; W02

International Patent Class (Main): H03H-007/09

File Segment: EPI

Manual Codes (EPI/S-X): U25-E02A; V01-B03D; V02-F01; V02-F03; W02-H

21/9/7 (Item 1 from file: 347)  
DIALOG(R)File 347:JAPIO  
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02893861 \*\*Image available\*\*  
IC PACKAGE

PUB. NO.: 01-191461 [JP 1191461 A]

PUBLISHED: August 01, 1989 (19890801)

INVENTOR(s): KANEKO TOMOYUKI

APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP

(Japan)  
APPL. NO.: 63-014741 [JP 8814741]  
FILED: January 27, 1988 (19880127)  
INTL CLASS: [4] H01L-025/00; H01L-023/06  
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)  
JOURNAL: Section: E, Section No. 839, Vol. 13, No. 483, Pg. 98,  
November 02, 1989 (19891102)

ABSTRACT

PURPOSE: To omit connection to an external capacitor, to remove high frequency noises and to implement high density mounting, by incorporating a bypass capacitor as a unitary body in an IC package, and connecting the capacitor between the power source pins of an IC element.

CONSTITUTION: An insulating film 7 comprising dielectric material is provided between metal films 6a and 6b which are connected to power source pins 5a and 5b. A parallel-plate capacitor is formed and made to be a bypass capacitor 8. The capacitor can be incorporated as a unitary body in a space 1a of a package 1. Connection can be performed at the closest position to an IC element 2. Frequency noises generated in the IC element 2 can be effectively removed.

?

29/9/1 (Item 1 from file: 2)

DIALOG(R) File 2:INSPEC

(c) 2004 Institution of Electrical Engineers. All rts. reserv.

7392803 INSPEC Abstract Number: A2002-21-8725D-007

Title: Capacitance steps and fusion pores of small and large-dense-core vesicles in nerve terminals

Author(s): Klyachko, V.A.; Jackson, M.B.

Author Affiliation: Dept. of Physiol., Wisconsin Univ., Madison, WI, USA

Journal: Nature vol.417, no.6893 p.89-92

Publisher: Nature Publishing Group,

Publication Date: 4 July 2002 Country of Publication: UK

CODEN: NATUAS ISSN: 0028-0836

SICI: 0028-0836(20020704)417:6893L.89:CSFP;1-M

Material Identity Number: N003-2002-027

U.S. Copyright Clearance Center Code: 0028-0836/02/\$12.00+2.00

Language: English Document Type: Journal Paper (JP)

Treatment: Experimental (X)

Abstract: The vesicles that package neurotransmitters fall into two distinct classes, large dense-core vesicles (LDCVs) and small synaptic vesicles, the coexistence of which is widespread in nerve terminals. High resolution capacitance recording reveals unitary steps proportional to vesicle size. Measurements of capacitance steps during LDCV and secretory granule fusion in endocrine and immune cells have provided important insights into exocytosis; however, extending these measurements to small synaptic vesicles has proven difficult. Here we report single vesicle capacitance steps in posterior pituitary nerve terminals. These nerve terminals contain neuropeptide-laden LDCVs, as well as microvesicles. Microvesicles are similar to synaptic vesicles in size, morphology and molecular composition, but their contents are unknown. Capacitance steps of two characteristic sizes, corresponding with microvesicles and LDCVs, were detected in patches of nerve terminal membrane. Both types of vesicles fuse in response to depolarization-induced Ca<sup>2+</sup> entry. Both undergo a reversible fusion process commonly referred to as 'kiss-and-run', but only rarely. Fusion pores seen during microvesicle kiss-and-run have a conductance of 19 pS, 11 times smaller than LDCV fusion pores. Thus, LDCVs and microvesicles use structurally different intermediates during exocytosis. (30 Refs)

Subfile: A

Descriptors: bioelectric phenomena; biological techniques; biomembrane transport; calcium; capacitance; molecular biophysics; neurophysiology

Identifiers: large-dense-core vesicle fusion pores; structurally different intermediates; nerve terminals; capacitance steps; exocytosis; posterior pituitary nerve terminals; molecular composition; nerve terminal membrane; depolarization-induced Ca<sup>2+</sup> entry; reversible fusion process; microvesicle kiss-and-run; neurotransmitters; small synaptic vesicles; high resolution capacitance recording; secretory granule fusion; endocrine cells; immune cells; Ca

Class Codes: A8725D (Biological transport; cellular and subcellular transmembrane physics); A8720E (Natural and artificial biomembranes); A8728 (Bioelectricity); A8730C (Electrical activity in neurophysiological processes); A8780 (Biophysical instrumentation and techniques)

Chemical Indexing:

Ca el (Elements - 1)

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29/9/2 (Item 1 from file: 34)

DIALOG(R) File 34:SciSearch(R) Cited Ref Sci

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04086009 Genuine Article#: RD213 Number of References: 27  
Title: THE IONIC CONDUCTANCE OF BARRIER ANODIC OXIDE-FILMS ON INDIUM  
Author(s): OMANOVIC S; METIKOSHUKOVIC M  
Corporate Source: UNIV ZAGREB, FAC CHEM ENGN & TECHNOL, DEPT  
ELECTROCHEM, SAVSKA C 16-I, POB 177/ZAGREB 41000//CROATIA/  
Journal: SOLID STATE IONICS, 1995, V78, N1-2 (MAY), P69-78  
ISSN: 0167-2738  
Language: ENGLISH Document Type: ARTICLE  
Geographic Location: CROATIA  
Subfile: SciSearch; CC PHYS--Current Contents, Physical, Chemical & Earth Sciences  
Journal Subject Category: PHYSICS, CONDENSED MATTER; CHEMISTRY, PHYSICAL  
Abstract: Formation and growth of thin anodic films on indium in a slightly alkaline borate buffer solution has been studied using galvanostatic and cyclic voltammetry techniques. In the galvanostatic conditions, oxide film growth occurs by activation-controlled ionic conduction by high electric field across the film, according to the exponential law. The following kinetic parameters of film growth have been examined: (i) the electric field strength, which is of the order of  $10(6)$  V cm $(-1)$ , (ii) the reciprocal capacity (the unitary formation rate), (iii) the constants A and B of the exponential law, (iv) the height of energy barrier for ion transport in the oxide phase, (v) the effective activation distance for the ionic jump over the energy barrier, and (vi) the pre-polarization oxide thickness. Using cyclic voltammetry, evidence has been given for primary passivation of indium in dynamic conditions. The oxide film formation process is under ohmic resistance control. The change in ohmic resistance is caused by the nucleation and spread of the oxide as a layer on the metal surface.  
Descriptors--Author Keywords: INDIUM ; IONIC CONDUCTION ; HIGH FIELD LAW ; VALVE METAL ; PASSIVITY ; ANODIZATION  
Identifiers--KeyWords Plus: TIN; GROWTH; MEDIA; KINETICS; BUFFER  
Research Fronts: 93-2142 001 (OXIDATION OF SILICON; FOURIER-TRANSFORM INFRARED ATTENUATED TOTAL REFLECTANCE SPECTROSCOPY; SEMICONDUCTOR SURFACES; ELECTROCHEMICAL INTERFACE)  
93-4904 001 (ANODIC ALUMINA FILMS; POROUS CERAMIC MEMBRANES; PASSIVE BEHAVIOR)  
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YOUNG L, 1961, ANODIC OXIDE FILMS

29/9/3 (Item 1 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
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013177720 \*\*Image available\*\*  
WPI Acc No: 2000-349593/200030  
Related WPI Acc No: 2000-349452; 2003-165492; 2003-439432  
XRAM Acc No: C00-106267  
XRXPX Acc No: N00-261920

Formation of a semiconductor structure for a semiconductor device includes forming a refractory metal within the recess, forming refractory metal nitride layers and forming a metallization layer to fill the recess

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)

Inventor: GIVENS J H; KRAUS B D; ZAHORIK R C

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6057231	A	20000502	US 97942811	A	19971002	200030 B
			US 99248499	A	19990210	

Priority Applications (No Type Date): US 97942811 A 19971002; US 99248499 A 19990210

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6057231	A	15	H01L-021/44	Div ex application	US 97942811

Abstract (Basic): US 6057231 A

NOVELTY - A semiconductor structure (10) is formed by forming a) a recess in the dielectric layer (14) on a substrate; b) a refractory metal layer (24) in the recess; c) a first refractory metal nitride layer (26) on the metal layer then heat treating the semiconductor substrate (12); d) a second refractory metal nitride layer (32) on the first; and e) a metallization layer to fill the recess.

USE - For forming a high aspect-ratio contact in a semiconductor device.

ADVANTAGE - The method forms a high aspect ratio structure that allows for taller microelectronic component i.e. taller stacked dynamic random access memory (DRAM) capacitor, where the interconnect to the stacked DRAM capacitor is unitary and formed by a single recess filling process.

DESCRIPTION OF DRAWING(S) - The figure shows an elevational cross-section illustration of the recess filling.

Semiconductor structure (10)  
Semiconductor substrate (12)  
Dielectric layer (14)  
Refractory metal layer (24)  
First refractory metal nitride layer (26)  
Second refractory metal nitride layer (32)  
pp; 15 DwgNo 6/7

Technology Focus:

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Method: Forming the refractory metal layer is conducted by a titanium chemical vapor deposition (CVD) process. Forming the second refractory metal nitride layer is conducted by a titanium nitride physical vapor deposition (PVD) process that causes titanium nitride to impact upon the first

refractory metal layer nitride at an angle that is orthogonal to the plane of the **semiconductor** substrate. The step of forming a metallization layer further comprises depositing an aluminum alloy composition to cover the recess at a deposition energy of 0.5-5 kW, preferably 5-20 kW and at 400-600degreesC, preferably 450-650degreesC; and applying for 1-500 seconds a pressure of 450-1,050 atmospheres and a temperature of 100-700degreesC. Heat treating step is conducted at 100-660degreesC for 10-60 seconds. Treating the **semiconductor** substrate with ammonia is conducted while heating the substrate at 100-500degreesC, preferably greater 200-400degreesC. The precleaning is conducted at 100:1 aqueous HF dip for 30 seconds. Preferred Property: The titanium nitride layer formed is 1,500-2,500 Angstrom, preferably 100-500 Angstrom thick. The layer of aluminum or aluminum alloy is 1.0-2.0um, preferably 0.5-2.0 um. The refractory metal layer is 100-300Angstrom thick. Preferred Compound: The titanium nitride CVD process uses tetrakis (dimethylamino) titanium (TDMAT) or trimethylethylenediamine tris (dimethylamino) titanium (TMEDT).

ELECTRONICS - Preferred Property: The recess has a height to width ratio of 6:1-10:1 and an opening of at most 0.35 mum at a top surface of the dielectric layer. The width of the trench opening wider or at most that of the contact hole opening and the length of the trench is parallel to the **semiconductor** substrate that exceeds the width of the contact hole opening. Preferred Method: Heat treating is conducted by rapid thermal processing (RTP) annealing.

Extension Abstract:

EXAMPLE - In an EMBODIMENT of the invention, the method includes performing a precleaning operation by subjecting the substrate to a hydrogen fluoride (HF) composition, and performing a degassing operation by subjecting the substrate to a vacuum. A first refractory metal nitride layer is formed within the recess upon the refractory metal layer by a titanium nitride CVD process using trimethylethylenediamine tris (dimethylamine) titanium (TMEDT). The substrate is treated with ammonia to replace interstitial impurities in the refractory metal nitride layer with nitrogen.

Title Terms: FORMATION; **SEMICONDUCTOR** ; STRUCTURE; **SEMICONDUCTOR** ; DEVICE ; FORMING; REFRACTORY; METAL; RECESS; FORMING; REFRACTORY; METAL; NITRIDE ; LAYER; FORMING; METALLISE; LAYER; FILL; RECESS

Derwent Class: L03; U11

International Patent Class (Main): H01L-021/44

International Patent Class (Additional): H01L-021/44

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L04-C10F

Manual Codes (EPI/S-X): U11-C05

Derwent Registry Numbers: 1712-U; 1713-U; 1738-U

29/9/4 (Item 2 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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010779223 \*\*Image available\*\*

WPI Acc No: 1996-276176/199628

XRPX Acc No: N96-232379

**Ferro-ceramic semiconductor capacitor - has parallelepiped whose internal volume is filled with high conductivity semiconductor formed by ferro-ceramic annealing in hydrogen**

Patent Assignee: LENGD POZITRON SCI PRODN ASSOC (LEPO-R)

Inventor: GALLAI I YA; ROTENBERG B A; SMIRNOV V F

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
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RU 2047925 C1 19951110 SU 4889290 A 19901207 199628 B

Priority Applications (No Type Date): SU 4889290 A 19901207

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
RU 2047925	C1	6	H01G-004/12	

Abstract (Basic): RU 2047925 C

Capacitor is made in the form of a parallelepiped whose internal volume is filled with high conductivity semiconductor (1) formed by ferro-ceramic annealing in the atmosphere of hydrogen. The edge external surface is formed by a thin dielectric layer (2) characterised by high dielectric permeability produced during the process of reoxidation annealing. Metallic electrodes (4) with the contacts (5) are applied on all the block surfaces except the narrow strip (3). The slot (6) acts as the interelectrode gap separating the block capacitors. Unitary capacitors are produced by separating the block into equal parts in the direction of the slot (6). Metallic electrodes are produced by annealing of silver paste or spraying it on and have symmetrical mutual arrangement.

USE/ADVANTAGE - Capacitor is used in radio-electronics. Its per unit volume capacitance is increased and the loss tangent is reduced.

Dwg.1,2/4

Title Terms: FERRO; CERAMIC; SEMICONDUCTOR ; CAPACITOR; PARALLELEPIPED; INTERNAL; VOLUME; FILLED; HIGH; CONDUCTING; SEMICONDUCTOR ; FORMING; FERRO; CERAMIC; ANNEAL; HYDROGEN

Derwent Class: V01

International Patent Class (Main): H01G-004/12

File Segment: EPI

Manual Codes (EPI/S-X): V01-B03A; V01-B03C5; V01-B03D1A

29/9/5 (Item 3 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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009421019 \*\*Image available\*\*

WPI Acc No: 1993-114533/199314

XRPX Acc No: N94-093048

High speed semiconductor integrated circuit - has cascaded inverters consisting of MOS transistors with input and output load capacitances satisfying given relationship

Patent Assignee: NEC CORP (NIDE )

Inventor: AIZAKI S

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 5055485	A	19930305	JP 91212557	A	19910826	199314 B
US 5305257	A	19940419	US 92935208	A	19920826	199415

Priority Applications (No Type Date): JP 91212557 A 19910826

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 5055485	A	5	H01L-027/088	
US 5305257	A	6	G11C-013/00	

Abstract (Basic): JP 5055485 A

Dwg.1/2

US 5305257 A

The size of an input side MOS transistor and that of an output side

MOS transistor of each inverter (IV) are determined so that an input capacitance ( $CG_j$ ) and an output load capacitance ( $CL_j$ ) of each inverter satisfy the following relationships.

$F_j = (CG(j+1) + CL_j) / CG_j$  and  $F(j+1) = F_j - (CL_j / CG_j)$ , where  $j$  is an integer having a value in a range between 1 and  $n$ , the number of inverters also being  $n$ , and  $F_j$  and  $F(j+1)$  are fan out of  $(j)$ th unitary circuits.  $CG_j$  is the input capacitance of each unitary circuit.

(First major country equivalent to JP5055485A)

Dwg.1/2

Title Terms: HIGH; SPEED; SEMICONDUCTOR ; INTEGRATE; CIRCUIT; CASCADE; INVERTER; CONSIST; MOS; TRANSISTOR; INPUT; OUTPUT; LOAD; CAPACITANCE; SATISFY; RELATED

Derwent Class: U13; U21

International Patent Class (Main): G11C-013/00; H01L-027/088

International Patent Class (Additional): H01L-021/82; H01L-027/10

File Segment: EPI

Manual Codes (EPI/S-X): U13-C02A; U13-B02A; U13-C02; U21-C01B3; U21-C03A1

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Designated States (National): IL JP  
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU  
MC NL PT SE  
EP 935812 A1 E H01J-035/16 Based on patent WO 9912183  
Designated States (Regional): DE FR NL  
JP 2001505359 W 20 H01J-035/16 Based on patent WO 9912183  
IL 129279 A H01J-035/16 Based on patent WO 9812183

Abstract (Basic): US 5802140 A

The apparatus has a unitary cylindrical vacuum enclosure (10) with an opening (15) in a top wall. The top and side walls of the enclosure are made of materials capable of providing a required radiation shielding. An anode assembly (12) has a rotating anode target (16) positioned within the enclosure and has a thermal capacity that is substantially smaller than that of the enclosure.

A cathode assembly (14) is spaced from and has an electron source (24) which emits electrons to strike the rotating anode target and generate X-rays to be released through an x-ray window of the enclosure. A mounting structure (22) holds the electron source, and a disk (28) is attached to the mounting structure facing the anode target shielding the opening the top wall of the enclosure against the X-rays. The disk is thermally coupled to the vacuum enclosure.

ADVANTAGE - Serves as a radiation shield, a heat reservoir for balancing the temperature within the vacuum enclosure in case of power loss and as direct heat transfer element between anode assembly and an air cooling system.

Dwg.1/4

Title Terms: X-RAY; GENERATE; APPARATUS; ROTATING; ANODE; HIGH; THERMAL; CAPACITY; UNIT; VACUUM; ENCLOSE; POSITION; DISC; THERMAL; COUPLE; ENCLOSE ; SHIELD; OPEN; TOP; WALL

Derwent Class: V05

International Patent Class (Main): H01J-035/06; H01J-035/16

International Patent Class (Additional): H01J-035/00

File Segment: EPI

Manual Codes (EPI/S-X): V05-E01B5; V05-E01E1; V05-E01F; V05-E01H1

26/9/13 (Item 1 from file: 347)

DIALOG(R) File 347:JAPIO

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02893861 \*\*Image available\*\*

IC PACKAGE

PUB. NO.: 01-191461 [JP 1191461 A]  
PUBLISHED: August 01, 1989 (19890801)  
INVENTOR(s): KANEKO TOMOYUKI  
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)  
APPL. NO.: 63-014741 [JP 8814741]  
FILED: January 27, 1988 (19880127)  
INTL CLASS: [4] H01L-025/00; H01L-023/06  
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)  
JOURNAL: Section: E, Section No. 839, Vol. 13, No. 483, Pg. 98, November 02, 1989 (19891102)

#### ABSTRACT

PURPOSE: To omit connection to an external capacitor, to remove high frequency noises and to implement high density mounting, by incorporating a bypass capacitor as a unitary body in an IC package, and connecting the

capacitor between the power source pins of an IC element.

CONSTITUTION: An insulating film 7 comprising dielectric material is provided between metal films 6a and 6b which are connected to power source pins 5a and 5b. A parallel-plate capacitor is formed and made to be a bypass capacitor 8. The capacitor can be incorporated as a unitary body in a space 1a of a package 1. Connection can be performed at the closest position to an IC element 2. Frequency noises generated in the IC element 2 can be effectively removed.

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